US-PAT-NO: 5846863

DOCUMENT-IDENTIFIER: US 5846863 A

TITLE: Method for manufacturing a semiconductor ROM device

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It is preferable that the second gate electrode is formed of polysilicon doped with an impurity or metal polycide. The first gate electrode can be also
formed of metal polycide, the second gate electrode can be formed of polysilicon doped with an impurity. Here, for a **metal of the metal silicide, a**
rare-earth metal such as tungsten (W), titanium (Ti), tantalum (Ta), or molybdenum (Mo) is used.

US-PAT-NO: 6491378

DOCUMENT-IDENTIFIER: US 6491378 B2

TITLE: Ink jet head, ink jet printer, and its driving method

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Where the terminal portions 10a, 101a and lead portions 10b, 101b are formed
of a **rare metal such as gold, platinum** or the like, it is possible to form a reliable electrode with an excellent corrosion resistance. On the other hand,
if these portions are formed of such a metal as aluminum having a high adhesion
to the glass substrate 4, it enables to manufacture the electrode inexpensively
and easily.

	L #	Hits	Search Text	DBs
1	L1	2	(("6303479") or ("6495882")).PN.	USPAT
2	L2	9	("4053924" | "4300158" | "4485550" | "5079182" | "5444302" | "5663584" | "5767557" | "5801398" | "6037605").PN.	USPAT
3	L3	0	6495882.URPN.	USPAT
4	L4	10	("4053924" | "4300152" | "4485550" | "4942441" | "5079182" | "5444302" | "5663584" | "5767557" | "5801398" | "6037605").PN.	USPAT
5	L5	143	schottky adj2 (source or drain)	USPAT
6	L6	3753	(source or drain) near10 silicide	USPAT
7	L7	31	5 and 6	USPAT
8	L8	4	(dielectric adj2 constant) and 7	USPAT
9	L9	264	(short-channel) near3 (mosfet or fet or mos)	USPAT
10	L10	8	5 and 9	USPAT
11	L11	132	schottky adj2 (source or drain)	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
12	L12	111	(short-channel) near3 (mosfet or fet or mos)	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

	L #	Hits	Search Text	DBs
13	L13	4	11 and 12	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

US-PAT-NO: 6486080

DOCUMENT-IDENTIFIER: US 6486080 B2

TITLE: Method to form zirconium oxide and hafnium oxide for high dielectric constant materials

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Semiconductor devices such as field effect transistors (FET) and random access memories (RAM) are common in the microelectronics industry. Performance of a MOSFET device can be enhanced in several ways. For example, the length of the gate electrode may be reduced. Alternatively, the thickness of the gate dielectric can be reduced. Either way, the MOSFET device performs faster.

In W. Qi et al, "MOSCAP and MOSFET characteristics using ZrO.sub.2 gate dielectric deposited directly on Si, IEDM Technical Digest, pp.145-148, (1999), and in B. Lee et al, "Ultra thin hafnium oxide with low leakage and excellent reliability for alternative gate dielectric applications," IEDM Technical Digest, pp. 133-136, (1999), it is found that zirconium oxide (ZrO.sub.2) and hafnium oxide (HfO.sub.2) show promise for future gate dielectric applications. The stability of these materials on the silicon surface and the ability to form them without the need for an interface layer, such as silicate, makes zirconium oxide and hafnium oxide good candidates to replace silicon dioxide.

The embodiments disclose a method to form metal oxide and composite metal
oxide-silicon oxide dielectric layers in the manufacture of an integrated circuit device. The present invention, in two preferred embodiments, is applied in exemplary fashion to the formation of an MOS transistor and a DRAM
cell. It should be clear to those experienced in the art that the present invention can be applied and extended without deviating from the scope of the
present invention.

Of particular importance to the first embodiment of the present invention is
the deposition of a metal oxide layer 18 overlying the substrate 10. Referring
now to FIG. 2, a metal oxide layer 18 is deposited overlying the substrate 10 using a chemical vapor deposition (CVD) process. In this example, the metal oxide layer 18 will form a high dielectric constant material for the gate dielectric of the completed MOS transistor.

W. Qi et al. "MOSCAP and MOSFET characteristics using ZrO.sub.2 gate dielectric deposited directly on Si", IEDM Technical Digest, pp. 145-148, (1999).